WHAT IS CLAIMED IS:

1. Strobe receiver circuitry, comprising:

a) a counter, said counter updating a count in response to strobe edges of received strobe signals; and

b) counter control logic, said counter control logic enabling said counter before each strobe signal is received by generating control signals asynchronously with respect to said received strobe signals; and said counter control logic resetting said counter after each strobe signal is received by receiving feedback from said counter and, in response to said feedback, resetting said counter asynchronously with respect to said received strobe signals.

2. Strobe receiver circuitry as in claim 1, wherein said control signal is a fixed width pulse.

3. Strobe receiver circuitry as in claim 1, wherein said control signal comprises start and stop conditions.

4. Strobe receiver circuitry as in claim 3, wherein said start and stop conditions are, respectively, falling and rising signal edges.

5. Strobe receiver circuitry, comprising:

a) a counter, said counter updating a count in response to strobe edges of received strobe signals; and

b) counter control logic, said counter control logic enabling said counter before each strobe signal is received by generating start conditions asynchronously with respect to said received strobe signals; and said counter control logic resetting said counter after each strobe signal is received by i) receiving

feedback from said counter, ii) generating stop conditions, and iii) in response to said feedback and stop conditions, resetting said counter asynchronously with respect to said received strobe signals.

6. Strobe receiver circuitry as in claim 5, wherein each received strobe signal consists of a multiple of P strobe edges ($P \geq 2$), and wherein:
   a) said counter is a rollover counter counting to P; and
   b) said counter control logic generates said stop conditions during receipt of a last P strobe edges of each strobe signal.

7. Strobe receiver circuitry as in claim 6, wherein:
   a) said counter control logic expects said counter to receive each strobe signal at a time falling between an early receipt case and a late receipt case; and
   b) said counter control logic generates said stop condition at a time falling between when said counter control logic expects said counter to receive:
      i) a first of a last P strobe edges of said late receipt case; and
      ii) a last strobe edge of said early receipt case.

8. Strobe receiver circuitry as in claim 6, wherein:
   a) said counter control logic expects said counter to receive each strobe signal at a time falling between an early receipt case and a late receipt case; and
   b) said counter control logic generates said stop condition at a time falling between:
      i) when said counter control logic expects said counter to receive a first of a last P strobe edges of said late receipt

case; and

ii) an end of a postamble following said early receipt case.

9. Strobe receiver circuitry as in claim 5, wherein said start and stop conditions are generated on a single signal line.

10. Strobe receiver circuitry as in claim 5, wherein:

a) said counter is a rollover counter comprising first and second state elements which are respectively and alternately clocked by rising and falling edges of received strobe signals; and

b) said counter control logic comprises first and second logic gates,

i) said first logic gate enabling and resetting said first state element in response to feedback from said first state element, said start condition, and said stop condition; and

ii) said second logic gate enabling and resetting said second state element in response to feedback from said first and second state elements.

11. Strobe receiver circuitry as in claim 10, wherein:

i) said first state element is a toggle flip-flop producing outputs SA and SA';

ii) said second state element is a toggle flip-flop producing outputs SB and SB';

iii) said first state element receives a reset input representing a logical AND of SA' and a single signal line on which said start and stop conditions are generated; and

iv) said second state element receives a reset input representing a logical AND of SA' and SB'.

12. Memory controller receiver circuitry, comprising:

a) a data pad and a strobe pad;

b) P storage elements coupled to receive data from said data pad ($P \geq 2$), said P storage elements being controlled by respective values of a count;

c) a counter, said counter updating said count in response to strobe edges of received strobe signals; and

d) counter control logic, said counter control logic enabling said counter before each strobe signal is received by generating control signals asynchronously with respect to said received strobe signals; and said counter control logic resetting said counter after each strobe signal is received by receiving feedback from said counter and, in response to said feedback, resetting said counter asynchronously with respect to said received strobe signals.

13. Memory controller receiver circuitry as in claim 12, wherein said control signal is a fixed width pulse.

14. Memory controller receiver circuitry as in claim 12, wherein said control signal comprises start and stop conditions.

15. Memory controller receiver circuitry as in claim 14, wherein said start and stop conditions are, respectively, falling and rising signal edges.

16. Memory controller receiver circuitry, comprising:

a) a data pad and a strobe pad;

b) P storage elements coupled to receive data from said data pad ($P \geq 2$), said P storage elements being controlled by respective

values of a count;

c) a counter, said counter updating said count in response to strobe edges of strobe signals received at said strobe pad; and

d) counter control logic, said counter control logic enabling said counter before each strobe signal is received by generating start conditions asynchronously with respect to said received strobe signals; and said counter control logic resetting said counter after each strobe signal is received by i) receiving feedback from said counter, ii) generating stop conditions, and iii) in response to said feedback and stop conditions, resetting said counter asynchronously with respect to said received strobe signals.

17. Memory controller receiver circuitry as in claim 16, wherein said counter control logic generates said stop condition at a time which is defined by whether a next read cycle will be:

a) a double data rate burst of four read cycle; or

b) a double data rate burst of eight read cycle.

18. Memory controller receiver circuitry as in claim 16, wherein said counter control logic generates said stop condition at a time which is defined by whether a next read cycle will be:

a) a 1x mode double data rate read cycle; or

b) an Mx mode double data rate read cycle ($M \geq 2$).

19. Memory controller receiver circuitry as in claim 16, wherein each received strobe signal consists of a multiple of P strobe edges, and wherein:

a) said counter is a rollover counter counting to P; and

b) said counter control logic generates said stop condition during

receipt of a last P strobe edges of each strobe signal.

20. Memory controller receiver circuitry as in claim 19, wherein:

a) said counter control logic expects said counter to receive each strobe signal at a time falling between an early receipt case and a late receipt case; and

b) said counter control logic generates said stop condition at a time falling between when said counter control logic expects said counter to receive:

i) a first of a last P strobe edges of said late receipt case; and

ii) a last strobe edge of said early receipt case.

21. Memory controller receiver circuitry as in claim 19, wherein:

a) said counter control logic expects said counter to receive each strobe signal at a time falling between an early receipt case and a late receipt case; and

b) said counter control logic generates said stop condition at a time falling between:

i) when said counter control logic expects said counter to receive a first of a last P strobe edges of said late receipt case; and

ii) an end of a postamble following said early receipt case.

22. Memory controller receiver circuitry as in claim 16, wherein said start and stop conditions are generated on a single signal line.

23. Memory controller receiver circuitry as in claim 16, wherein:

a) said counter is a rollover counter comprising first and second state elements which are respectively and alternately clocked

by rising and falling edges of strobe signals received at said strobe pad; and

b) said counter control logic comprises first and second logic gates,

i) said first logic gate enabling and resetting said first state element in response to feedback from said first state element, said start condition, and said stop condition; and

ii) said second logic gate enabling and resetting said second state element in response to feedback from said first and second state elements.

24. Memory controller receiver circuitry as in claim 23, wherein said rollover counter comprises P AND gates, each of which receives a different combination of outputs from said first and second state elements, and each of which produces one bit of a P bit, one-high count, the bits of which respectively control ones of said P storage elements.

25. Memory controller receiver circuitry as in claim 23, wherein:

i) said first state element is a toggle flip-flop producing outputs SA and SA';

ii) said second state element is a toggle flip-flop producing outputs SB and SB';

iii) said first state element receives a reset input representing a logical AND of SA' and a single signal line on which said start and stop conditions are generated; and

iv) said second state element receives a reset input representing a logical AND of SA' and SB'.

26. Memory controller receiver circuitry as in claim 25, wherein said rollover counter comprises P AND gates which:

    i) respectively receive flip-flop outputs SA' and SB', SA and SB', SA and SB, and SA' and SB; and

    ii) respectively produce one bit each of a P bit, one-high count, the bits of which respectively control ones of said P storage elements.

27. Memory controller receiver circuitry as in claim 16, wherein P=4.

28. A double data rate memory controller with tolerance for large variation in read loop delay, comprising:

    a) data receiving means;

    b) counting means for receiving and counting a number of strobe edges received during a memory read cycle;

    c) means for controlling said data receiving means in response to a count produced by said counting means; and

    d) means for enabling said counting means before each memory read cycle and resetting said counting means after each memory read cycle by i) enabling said counting means asynchronously with respect to said number of strobe edges, and ii) resetting said counting means asynchronously with respect to said number of strobe edges.

29. A method of receiving strobe signals into a memory controller, comprising:

    a) enabling a strobe edge counter asynchronously with respect to said strobe signals, before each strobe signal is received, and in response to a start condition; and

    b) resetting said strobe edge counter asynchronously with respect

to said strobe signals, after each strobe signal is received, and in response to a combination of counter feedback and a stop condition.

30. A method as in claim 29, wherein each received strobe signal consists of a multiple of P strobe edges ($P \geq 2$), and wherein said counter is a rollover counter counting to P, the method further comprising:

generating said stop condition during receipt of a last P strobe edges of each strobe signal.

31. A method as in claim 30, wherein said counter receives each strobe signal at a time falling between an early receipt case and a late receipt case, the method further comprising:

generating said stop condition at a time falling between when said counter is expected to receive:

i) a first of a last P strobe edges of said late receipt case; and

ii) a last strobe edge of said early receipt case.

32. A method as in claim 30, wherein said counter receives each strobe signal at a time falling between an early receipt case and a late receipt case, the method further comprising:

generating said stop condition at a time falling between:

i) when said counter is expected to receive a first of a last P strobe edges of said late receipt case; and

ii) an end of a postamble following said early receipt case.

33. A method of receiving data into a memory controller, comprising, during a memory read cycle:

a) enabling a counter asynchronously with respect to a strobe

signal, before the strobe signal is received at a strobe pad, and in response to a start condition;

b) storing respective data bits received at a data pad in P storage elements ($P \geq 2$), in response to a count produced by said counter; and

c) resetting said counter asynchronously with respect to said strobe signal, after the strobe signal is received, and in response to a combination of counter feedback and a stop condition.

34. A method as in claim 33, further comprising resetting said counter at different times, depending on whether a memory read cycle is:

a) a double data rate burst of four read cycle; or

b) a double data rate burst of eight read cycle.

35. A method as in claim 33, further comprising resetting said counter at different times, depending on whether a memory read cycle is:

a) a 1x mode double data rate read cycle; or

b) a 2x mode double data rate read cycle.

36. A computer system, comprising:

a) a CPU;

b) a memory controller coupled to said CPU;

c) an I/O controller coupled to said CPU;

d) a number of I/O devices coupled to said I/O controller; and

e) a number of memory modules coupled to said memory controller;

wherein said memory controller comprises a plurality of data and strobe pads to which are coupled receiver circuitry for receiving data and strobe signals from said memory modules; and

wherein said receiver circuitry comprises, for corresponding data and strobe pads:

i) P storage elements coupled to receive data from said data pad ($P \geq 2$), said P storage elements being controlled by respective values of a count;

ii) a counter, said counter updating said count in response to strobe edges of strobe signals received at said strobe pad; and

iii) counter control logic, said counter control logic enabling said counter before each strobe signal is received by generating start conditions asynchronously with respect to said received strobe signals; and said counter control logic resetting said counter after each strobe signal is received by i) receiving feedback from said counter, ii) generating stop conditions, and iii) in response to said feedback and stop conditions, resetting said counter asynchronously with respect to said received strobe signals.

37. A computer system as in claim 36, wherein each of said P storage elements is a latch.

38. A computer system as in claim 36, wherein said count is a P-bit, one-high count, the bits of which respectively control ones of said P storage elements.

39. A computer system as in claim 36, wherein said memory controller and said I/O controller form an integrated memory and I/O controller.

40. A computer system as in claim 36, wherein said start and stop

conditions are generated on a single signal line.

41. A computer system as in claim 36, wherein:

a) said counter is a rollover counter comprising first and second state elements which are respectively and alternately clocked by rising and falling edges of strobe signals received at said strobe pad; and

b) said counter control logic comprises first and second logic gates,

i) said first logic gate enabling and resetting said first state element in response to feedback from said first state element, said start condition, and said stop condition; and

ii) said second logic gate enabling and resetting said second state element in response to feedback from said first and second state elements.

42. A computer system as in claim 41, wherein said rollover counter comprises P AND gates, each of which receives a different combination of outputs from said first and second state elements, and each of which produces one bit of a P bit, one-high count, the bits of which respectively control ones of said P storage elements.